Amendments to the Claims

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Canceled)

22. (Currently Amended) A switched capacitor circuit, comprising:

an integrator;

a summing junction switch connected to said integrator;

a sampling capacitor connected to said summing junction switch;

a signal conducting MOSFET switch connected to said sampling capacitor; and

a replica network that controls a resistance of said signal conducting MOSFET switch in response to variations in an input signal voltage received at said signal conducting MOSFET switch, said replica network connected to a gate terminal of said signal conducting MOSFET switch.

23. (Original) The switched capacitor circuit of claim 22, wherein said integrator is a differential integrator and said summing junction switch is connected to an inverting terminal of said differential integrator.

24. (Currently Amended) The switched capacitor circuit of claim 23, further comprising:

a second summing junction switch connected to a noninverting terminal of said differential integrator;

a second sampling capacitor connected to said second summing junction switch;

a second signal conducting MOSFET switch connected to said second sampling capacitor; and

a second replica network that controls a resistance of said second signal conducting MOSFET switch in response to variations in a second input signal voltage received at said second signal conducting MOSFET switch, said second replica network connected to a gate terminal of said second signal conducting MOSFET switch.

25. (Canceled)

26. (Canceled)

27. (Canceled)

28. (Canceled)

29. (Canceled)

30. (Canceled)

31. (Canceled)

32. (Canceled)

33. (Canceled)

34. (Canceled)

35. (Canceled)

36. (Canceled)

37. (Canceled)

38. (Canceled)

39. (New) A switched capacitor circuit, comprising:

an integrator;

a first switch connected to said integrator;

a first capacitor connected to said first switch;

a first field effect transistor connected to said first capacitor; and

a first network configured to control a resistance of said first field effect transistor in response to variations in a first input signal voltage received at said first field effect transistor, said first network connected to a gate terminal of said first field effect transistor.

40. (New) The switched capacitor circuit of claim 39, wherein said first network comprises:

a bridge circuit, wherein a second field effect transistor is disposed in a resistor branch of said bridge circuit; and

an operational amplifier, wherein a noninverting terminal of said operational amplifier is connected to a first node of said bridge circuit, an inverting terminal of said operational amplifier is connected to a second node of said bridge circuit, said second node is separated from said first node by a third node of said bridge circuit, an output of said operational amplifier is connected to a gate terminal of said second field effect transistor and to said gate terminal of said first field effect transistor.

41. (New) The switched capacitor circuit of claim 40, further comprising a second capacitor connected in parallel between said output of said operational amplifier and said second node.

42. (New) The switched capacitor circuit of claim 41, further comprising a second switch coupled between said output of said operational amplifier and said gate terminal of said first field effect transistor.

43. (New) The switched capacitor circuit of claim 42, further comprising a third switch coupled between a fourth node and a ground, wherein said fourth node is positioned between said second switch and said gate terminal of said first field effect transistor.

44. (New) The switched capacitor circuit of claim 39, wherein said integrator is a differential integrator.

45. (New) The switched capacitor circuit of claim 44, wherein said differential integrator comprises:

an operational amplifier;

a second capacitor coupled to an inverting terminal of said operational amplifier; and

a third capacitor coupled to a noninverting terminal of said operational amplifier.

46. (New) The switched capacitor circuit of claim 45, wherein said first switch is connected to said inverting terminal.

47. (New) The switched capacitor circuit of claim 45, further comprising:

a second switch connected to said noninverting terminal.

48. (New) The switched capacitor circuit of claim 47, further comprising:

a fourth capacitor connected to said second switch.

49. (New) The switched capacitor circuit of claim 48, further comprising:

a second field effect transistor connected to said fourth capacitor.

50. (New) The switched capacitor circuit of claim 49, further comprising:

a second network configured to control a resistance of said second field effect transistor in response to variations in a second input signal voltage received at said second field effect transistor, said second network connected to a gate terminal of said second field effect transistor.

51. (New) The switched capacitor circuit of claim 50, wherein said second network comprises:

a bridge circuit, wherein a third field effect transistor is disposed in a resistor branch of said bridge circuit; and

a second operational amplifier, wherein a noninverting terminal of said second operational amplifier is connected to a first node of said bridge circuit, an inverting

terminal of said second operational amplifier is connected to a second node of said bridge circuit, said second node is separated from said first node by a third node of said bridge circuit, an output of said second operational amplifier is connected to a gate terminal of said third field effect transistor and to said gate terminal of said second field effect transistor.

52. (New) The switched capacitor circuit of claim 51, further comprising a fifth capacitor connected in parallel between said output of said second operational amplifier and said second node.

53. (New) The switched capacitor circuit of claim 52, further comprising a third switch coupled between said output of said second operational amplifier and said gate terminal of said second field effect transistor.

54. (New) The switched capacitor circuit of claim 53, further comprising a fourth switch coupled between a fourth node and a ground, wherein said fourth node is positioned between said third switch and said gate terminal of said second field effect transistor.

This listing of claims will replace all prior versions, and listings of claims in the application.